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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,386	03/15/2004	Tongbi Jiang	500180.03 (29249/US/2)	3160

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EXAMINER	
LOUIE, WAI SING	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,386	JIANG, TONGBI	
	Examiner	Art Unit	
	Wai-Sing Louie	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34,36,37,42,44 and 45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34,36,37,42,44 and 45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 34 is rejected under 35 U.S.C. 102(b) as being anticipated by Sachdev et al. (US 5,773,561), new cited.

With regard to claim 34, Sachdev et al. disclose a epoxy based adhesive for semiconductor chip attachment (col. 3, line 45 et seq.), comprising:

- A semiconductor chip (col. 1, lines 14-17);
- A substrate to which the semiconductor chip is attached (col. 2, lines 22-36);
- A tri-layer die attach tape (col. 4, lines 27-35) comprising adhesive die attach material (siloxane) disposed between the semiconductor die and the substrate, the adhesive die attach material directly abutting the substrate and the semiconductor die (col. 2, lines 22-36), a die attach bondline at the interface between the adhesive die attach material and the semiconductor die being substantially void free (col. 4, lines 27-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 36-n are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachdev et al. (US 5,773,561) in view of Conru et al. (US 5,086,018).

With regard to claims 36 and 44, Sachdev et al. do not disclose a lead frame disposed between the semiconductor chip and the substrate. However, Sachdev et al. disclose the problem of the chip interface with the wiring (col. 1, lines 52-54) and Conru et al. disclose the lead frame 14 is disposed in between the semiconductor chip 12 and the substrate 18 (Conru fig. 2 and 3). Conru et al. teach the tri-layer tape helps assure that short circuits between the lead frame and the chip do not occur (Conru col. 3, lines 18-20). Therefore, it would have been obvious to one of ordinary skill in the art to modify Sachdev's device with the teaching of Conru et al. to provide a tri-layer die attach tape in order to assure that short circuits between the lead frame and the chip do not occur.

With regard to claims 37 and 45, Sachdev et al. disclose the adhesive die attach material is conductive adhesive (col. 3, lines 28-32) and therefore, Sachdev et al. modified by Conru et al. in claim 36 above, the semiconductor chip 12 would be electrically coupled to the conductive trace 14 formed on the surface of the substrate 18 through conductive bond wires 16 (Conru fig. 3).

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sachdev et al. (US 5,773,561) modified by Conru et al. (US 5,086,018) as applied to claim 36 above, and further in view of Desai et al. (US 6,266,249).

With regard to claim 42, in addition to the limitations disclosed in claim 34 above, Sachdev et al. modified by Conru et al. also disclose:

- A pressure and heat cured adhesive die attach material disposed between the semiconductor chip and the first surface of the substrate being substantially void free (col. 10, lines 17-33);
- A plurality of bond pads 53 disposed on the semiconductor die 52, the bond pads 53 being electrically coupled to a corresponding plurality of conductive leads 51 on the second surface of the substrate 57 by the bond wire 54 (Conru fig. 5). Sachdev et al. modified by Conru et al. do not disclose the aperture on substrate 57 and where the bond pads aligned with and bond wires passing through. However, Desai et al. disclose through holes 18 on the substrate 22, where the semiconductor device 30 aligned the through holes 18 (Desai col. 3, lines 51-64) and conductive traces 24 are electrically coupled the via 18 by solder (Desai col. 3, lines 40-49). Desai teaches the IC device can be miniaturized by stacking the devices and connecting with through holes (Desai col. 1, lines 18-22 and lines 39-43). Therefore, it would have been obvious to one of ordinary skill in the art to modify Sachdev's device with the teaching of Conru et al. and Desai et al. to provide a substrate with apertures in order to stack the devices and connect with through holes.

Response to Arguments

Applicant's arguments with respect to claims 34, 36-37, 42, and 44-45 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wai-Sing Louie whose telephone number is (571) 272-1709. The examiner can normally be reached on 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WAI SING LOUIE
PRIMARY PATENT EXAMINER

Wsl
November 7, 2006.